Interposer-to-Interposer Electrical and Silicon Photonic Interconnection Platform using Silicon Bridge

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Introduction

Developing solutions that provide high-bandwidth and low-energy communication has been at the forefront of interconnect and packaging research [1]. Within a module, the challenge has been addressed by using novel 2.5D (silicon interposer) and 3D stacking for short and high-density electrical interconnections and silicon photonics based interconnects. However, wafer-level batch fabricated solutions for high-bandwidth and low-energy interconnection between modules remain largely missing. Fig. 1 illustrates three approaches for package-to-package communication: through the motherboard, Flex connection [2], and using optical fibers. Electrical connectivity through the motherboard is both bandwidth limited and energy consuming. The use of Flex connection provides lower loss channels, however it requires a serial assembly process, which may limit its scalability. Methods involving optical fibers suffer the same limitation and are limited to relatively large interconnect pitches.

Interconnect Platform Description

In this work, we describe a novel interconnection platform involving multiple silicon interposer "tiles" (Fig. 2 and Fig. 3). Each tile contains one or more chips or stacks of chips on the top surface. Each tile also contains both multiple dense metallization layers for within interposer electrical interconnection as well as silicon nanophotonic waveguides.

The tiles are aligned and mounted directly on the FR4 PWB using positive self-alignment structures (PSAS) and inverted pyramid pits (Fig. 4). Four pits are fabricated near the corners of the tiles, and four PSAS are fabricated on the PWB in positions corresponding to the pits. The alignment is induced when tiles and PWB are brought close together; as much as 150 µm of misalignment can be corrected once some force is applied on the tiles to be mounted on the PWB. As small as 1 µm accuracy can be achieved for silicon-to-silicon alignment, while <5 µm accuracy can be achieved for silicon-to-FR4 alignment.

Communication between the tiles occurs through a silicon-based bridge; the PWB is primarily used for mechanical support and to provide I/Os to the entire system. The bridge is designed to provide both dense electrical and silicon nanophotonic interconnections. Using the PSAS technology, the silicon-based bridge is aligned and assembled on top of the tiles, and each bridge is positioned to span two or more tiles that it is intended to interconnect.

It is critical that the tiles and the bridges are assembled and interconnected using non-permanent means; this enables replacement of defective or malfunctioning tiles and bridges even after the testing phase. This is particularly important as systems become increasingly large, which increases components that are subject to yield.

To this end, dense electrical interconnections are provided using mechanically flexible interconnects (MFIs), which are batch fabricated at the wafer level (Fig. 5 and Fig. 6). Each MFI is capable of bending vertically up to 65 µm, and the FEM-engineered shape ensures that the structure remains in the elastic regime. The vertical compliance, along with the "pointy" shape of the MFIs, enables low-resistance electrical contact that can be deformed multiple times. Four-point measurements performed on assembled MFI/pad pairs after 10 re-assembly steps show unchanged low resistance (from 103 mΩ to 105 mΩ). In addition, MFIs can be used to interconnect silicon tiles and the PWB, where the vertical compliance can be leveraged to compensate for surface non-planarity (Fig. 6).

Nanophotonic interconnections are provided through proximity coupling between tiles and bridges; both grating couplers and silicon mirrors can be used [1]. However, the coupling efficiency depends strongly on the alignment accuracy, and PSAS technology provides alignment accuracy of ~7 µm (worst case) in the configuration with FR4 PWB, tiles, and bridges. Higher level of alignment has been demonstrated.

Fig. 3 shows an assembled system that contains three tiles and two bridges. All tiles and bridges have been aligned using PSAS and without a placement tool. MFIs are also fabricated on top of the tiles, and electrical connectivity from tile #1 to tile #3 through two bridges has been demonstrated.

For the electrical interconnection, a comparison of the bandwidth density between interposers through the silicon bridge and the motherboard-level interconnects is shown in Fig 7; models from [3, 4] were used. The wire pitch on the bridge and motherboard are assumed to be 10 µm and 350 µm, respectively. For systems involving nanophotonics, the bridge enables higher bandwidth density between modules as the silicon waveguides (with couplers) can typically be fabricated with a pitch of less than 10 µm as opposed to the typical 250 µm pitch of optical fibers (Fig. 9); photonic interconnect models are adapted from [5].

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Reference

[1] A. Krishnamoorthy et al., *Proceedings of the IEEE* , vol. 97, no.7, July 2009. **[2]** F. O'Mahony et al, *IEEE J. Solid-state Circuits*, vol. 45, no. 12, Dec. 2010. **[3]** H. Cho, et al., *IEEE J. Light. Technol.*, vol. 22, no. 9, pp. 2021–2033, 2004. **[4]** V. Kumar, et al. in Proc. *IEEE Int. Interconnect Technol. Conf.*, pp. 1–3, 2013. **[5]** S. Rakheja et al., in Proc. *IEEE Int. Symp. On Quality Electronic Design*, pp.732,739, 2012.

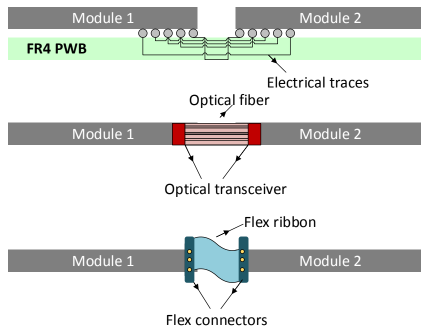

Fig. 1: Different methods of interconnecting high performance modules/packages

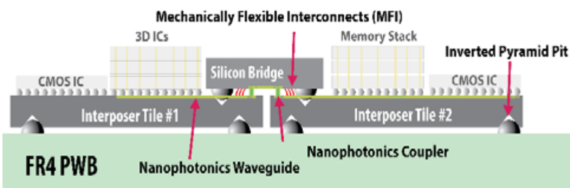

Fig. 2: Schematic of proposed platform in which interposer tiles are interconnected using electrical and photonic interconnects through the silicon bridge

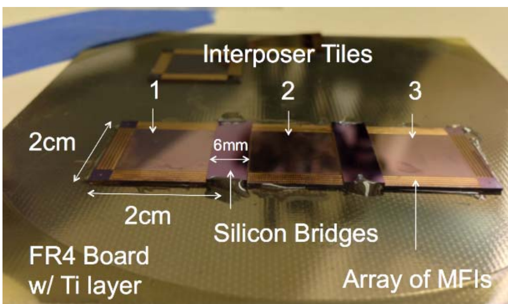

Fig. 3: Assembled interposer tiles with silicon bridges

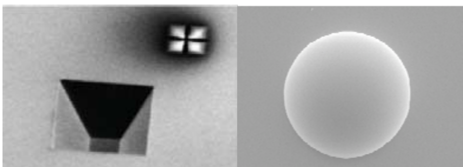

Fig. 4: SEM images of (a) pit and (b) PSAS

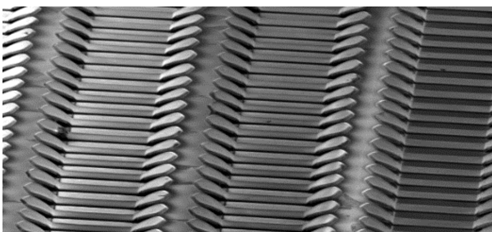

Fig. 5: SEM of dense MFIs between titles and bridge

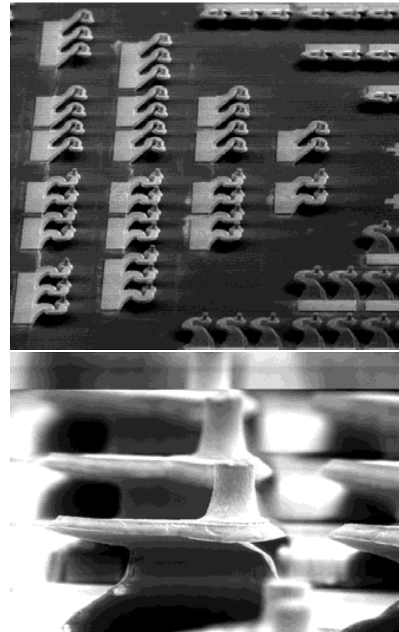

Fig. 6: SEM image of MFIs with a truncated-cone tip for interposer tile to motherboard assembly

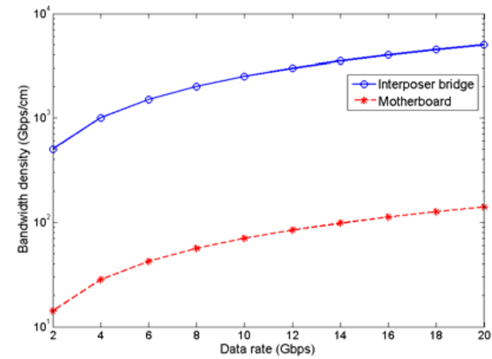

Fig. 7: Bandwidth density of (non-optimized) electrical interconnects on the bridge and the motherboard

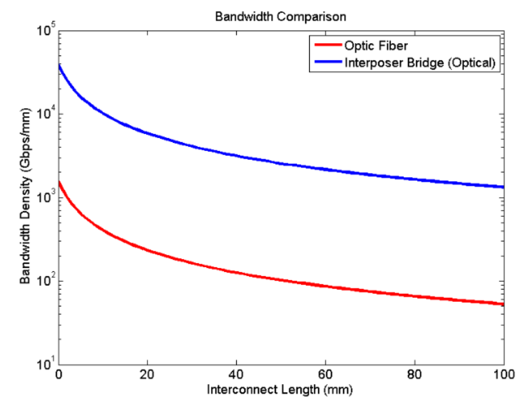

Fig. 8: Bandwidth density of optical fiber and bridge-level silicon photonic interconnects